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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL. NO.	FILING DATE	CLASS	SUBCLASS	CAV	EXAMINER
0024001	12/03/01	3-5		2818	10-1-0
Forbes Leonard; Eldridge Jerome; Ahn Kis;					
2818					
<p>**CONTINUING DATA VERIFIED:</p> <p>THIS APPLICATION IS A CIP OF 09/943;134/08/30/2001 TR</p>					
<p>**FOREIGN APPLICATIONS VERIFIED:</p>					
<p>DO NOT PUBLISH <input type="checkbox"/> REASON <input type="checkbox"/></p> <p>Foreign priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No</p> <p>USC 110 conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No</p> <p>Verified and Acknowledged Examiner's Initials: DR</p> <p>ATTORNEY DOCKET NO. 1303-035US1</p> <p>TITLE: Programmable array logic or memory with peripheral devices and asymmetrical tunnel barriers</p> <p>U.S. DEPT. OF COMM. PAT. & TM. PTO-4130 Rev. 12-94</p>					
FORMAL DRAWINGS					

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NOTICE OF ALLOWANCE MAILED		TU TR HO		CLAIMS ALLOWED	
11/19/03		Assistant Examiner 11/03		Total Claims 22	Print Claim for O.G. 1
ISSUE FEE		David Neils		DRAWING	
Amount Due \$1630	Date Paid	Supervisory Patent Examiner Technology Center 2800		Sheets Drwg. 17	Figs. Drwg. 24
		Primary Examiner		Print Fig. 3	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE		Application Examiner	
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